IXP12DE Intel® IXP1200 Network Processor Development Environment

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Product Highlights

IXP12DE Network Processor Development Environment

- Microengine programming and simulation environment
- Intel® StrongARM* processor simulation environment
- Integrated linker, loader, assembler, and debugger
- Integrated cycle- and data-accurate simulator of the IXP1200 Network Processor
- Windows NT* GUI
- Supports IXP12EB Evaluation Kit

Software Libraries

- Hardware Debug
- Route and Bridge Table Managers
- Device Drivers
- Sample Boot Code and Diagnostics

IX Bus Design Tools

- IBIS Models
- IX Bus Design Guide
- Verilog Models for the IXF440, IXF1002 and IXB3208 IX Bus peripheral chips (optional)

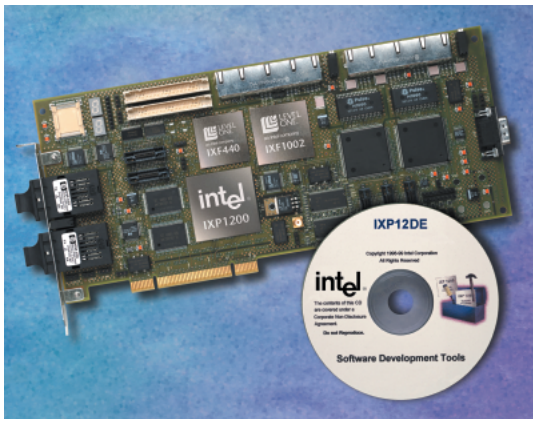
Product Overview

IXP1200 Network Processor Family

Intel's IXP1200 – the first true network processor – is the cornerstone of the Intel® Internet Exchange™ (IX) architecture. The IXP1200 Network Processor combines the best attributes of a custom network ASIC and an embedded microprocessor. It is the first device to combine an embedded microprocessor core with six multiple, scalable microengines. This highly integrated processor helps deliver the flexible programmability to satisfy rapidly changing requirements, together with high data-rate performance.

The IXP12DE Network Processor Development Environment is part of the growing family of products for the IXP1200 Network Processor, providing a feature-rich workbench that enables the fast time-to market development of networking products.

When used with IXP12EB Evaluation Kit, the



IXP12DE provides a comprehensive software-based development environment that developers can use to quickly build custom network processor-based applications and value-added features. Examples include Quality of Service (QoS) and advanced security applications that support the convergence of voice and data, in addition to LAN/WAN technologies.

One of the most significant attributes of the IXP1200 Network Processor is its ease of programmability. This promotes software-based product differentiation that can help minimize cost of ownership, shrink time-to-market, reduce development costs, and extend the life of network and telecommunications products.

Programming the IXP1200

By programming the IXP1200 Network Processor, developers can replace many functions that previously required time-consuming development in ASICs.

The IXP1200 Network Processor integrates six programmable, multithreaded microengines, each supporting four independent execution threads. The IXP12DE development environment provides an integrated, easy-to-use workbench for the efficient development of applications for both the Network Processor's Intel StrongARM core and the microengines. A user-friendly graphical user interface (GUI) simplifies writing, assembling, and optimizing symbolic microcode and facilitates the task of building, simulating, and debugging custom IXP1200 Network Processor configurations.

IXP1200 Microengines Instruction Set

This microcode is specifically designed for network data traffic. It provides an optimal level of abstraction for hardware control and software programming to speed the development of feature-rich and highly differentiated network equipment. Additional features, such as automatically assigning symbolic variables, or instructing the assembler to perform hardware optimization, are ideal for shortening product development cycles.

Name	Description
ARITHMETIC, ROTATE, AND SHIFT INSTRUCTIONS	
ALU	Perform ALU Operation
ALU_SHF	Perform ALU and shift operation
DBL_SHIFT	Join 2 longwords, shift, save longword
BRANCH AND JUMP INSTRUCTIONS	
BR, BR=0, BR!=0	Branch on condition code
BR>0, BR<0	Branch on condition code
BR>=0, BR<=0	Branch on condition code
BR=count, BR!=count	Branch on condition code
BR_BSET, BR_BCLR	Branch on bit set or bit clear
BR=BYTE, BR!=BYTE	Branch on byte equal
BR=CTX, BR!=CTX	Branch on current context
BR_INP_STATE	Branch on event state
BR_!SIGNAL	Branch if signal disasserted
JUMP	Jump to label
RTN	Return from branch or jump
READ/WRITE INSTRUCTIONS	
CSR	Reference a control/status signal
FAST_WR	Write immediate data to CSRs
LOCAL_CSR_RD	Read CSR
LOCAL_CSR_WR	Write CSR
R_FIFO_RD	Read the receive FIFO buffer

Name	Description
ARITHMETIC, ROTATE, AND SHIFT INSTRUCTIONS	
T_FIFO_WR	Write to transmit FIFO buffer
PCI_DMA	Issue to PCI unit
SCRATCH	Read/write scratchpad RAM
SDRAM	Read/write SDRAM
SRAM	Read/write SRAM
LOCAL REGISTER INSTRUCTIONS	
FIND_BSET	Find first bit set in any 16-bit reg field
FIND_BSET_WITH_MASK	Find first bit set with mask
IMMED	Load immediate word, sign-extend, shift
IMMED_B0,IMMED_B1	Load immediate byte to a field
IMMED_B2,IMMED_B3	Load immediate byte to a field
IMMED_W0,IMMED_W1	Load immediate word to a field
LD_FIELD	Load byte(s) into specified field(s)
LD_FIELD_W_CLR	Load byte(s) into specified field(s)
LOAD_ADDR	Load instruction address
LOAD_BSET_RESULT1	Load result of FIND_BSET instruction
LOAD_BSET_RESULT2	Load result of FIND_BSET_MASK
MISCELLANEOUS INSTRUCTIONS	
CTX_ARB	Swap contexts and wake on event
HASHx_48	Perform 48-bit hash(x=1,2,3)
HASHx_64	Perform 64-bit hash(x=1,2,3)
NOP	No operation

Packet Forwarding: Application Examples

The IXP12DE includes an example application code that demonstrates Layer 2 and Layer 3 bridging and routing, in three configurations. The reference design features generic scheduling and queuing mechanisms that can be readily extended or adapted to other protocols. Intel makes this microcode freely available to developers to promote a greater understanding of programming the IXP1200 Network Processor.

Example code configurations:

- 12-port 100 Mbps Fast Ethernet
- 16-port 100 Mbps Fast Ethernet
- 1-port 1 Gbps Fast Ethernet

IXP12DE Workbench

Features of the workbench include:

- Set Breakpoints
- Go/Go To/Step Navigation
- Data Watch Window
- Thread History Window
- Command Line Window
- Performance Statistics
- Save and Restore Simulation Session
- Memory Modify History

Building New Internet Applications

The IXP1200 Network Processor provides the scalable performance and programmability for designing a wide variety of intelligent, upgradable network and telecommunications equipment. Enterprise, access, and service provider/carrier applications that can benefit from this versatility include multi-service switches, routers and aggregation platforms; VPN, firewall and intrusion detection systems;VoIP gateways; and web switch appliances.

Feature-Rich Development Environment

FEATURES	BENEFITS
Portable Operating System Application Programming Interface (API)	Most of the IXP1200 Network Processor Application subsystems and libraries utilize ANSI C/C++ libraries. However, the few non-portable calls used are layered and isolated in a common library – common.lib – consisting of semaphores, threads, and system timer calls. This eases the task of porting subsystems and libraries to another operating system
IXP1200 HAL	Provides chip CSR memory mappings, timer interfaces, and board memory mappings
Microcode Loader	Loads microcode images, created by the microcode ucld linker, to the appropriate microengines
Microengine Debug Library	Enables debugging of non-StrongARM portions of the IXP1200 Network Processor
Communication Drivers	Allows hardware to communicate to the Network Processor workbench over RS232 serial lines and Ethernet
Microengine Driver	Handles communication between microprocessor core and microengines
PCI Device Driver	Enables communication with PCI devices
IX Bus Device Drivers	Manages devices on the IX Bus
Remote Access RPC	Implements standard Sun RPC
Library Dispatch	Converts inter-processor messages to and from application library function calls
Message Queue	Manages synchronous communications between system software and threads
Service Libraries	Enable an application to call microengine service routines, such as load hash multiplier, hash operation, scatter/gather and memory operation
Foreign Model Interface	Can interface to Verilog or VHDL environments
Example Network Application Code	Includes route table manager, bridge table manager, and initialization sequence to bring up actual hardware

A New Approach to Development

The Intel IX Architecture is a comprehensive family of feature-rich silicon and software building blocks and tools that accelerates development of powerful, flexible network and communications products. The cornerstone of the Intel Internet Exchange Architecture is the Intel IXP1200 network processor–which combines the performance and programmability to develop intelligent, differentiated network solutions–at the speed of Internet growth.

For more information on the family of network processor products, please visit http://developer.intel.com/design/network.

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